ABSTRACT OF THE DISCLOSURE

The invention includes a method for forming graded junction regions comprising: a) providing a semiconductor material wafer; b) providing a transistor gate over the semiconductor material wafer, the transistor gate having opposing lateral sidewalls; c) providing sidewall spacers adjacent the sidewalls of the transistor gate, the sidewall spacers having a lateral thickness; d) decreasing the lateral thickness of the sidewall spacers; and e) after decreasing the lateral thickness of the sidewall spacers, implanting a conductivity-enhancing dopant into the semiconductor material to form graded junction regions operatively adjacent the transistor gate. The invention also includes a semiconductor transistor device comprising: a) a region of a semiconductor material wafer; b) a transistor gate over a portion of the region of the semiconductor material wafer, the transistor gate having opposing lateral sidewalls; c) opposing source/drain regions operatively adjacent the transistor gate, each source/drain region having an inner lateral boundary; d) opposing sidewall spacers adjacent the sidewalls of the transistor gate, each sidewall spacer having an outer lateral edge, the sidewall spacers and source/drain regions being paired such that the outer lateral edges of the sidewall spacers are displaced laterally inwardly relative to the inner lateral boundaries of the source/drain regions; and e) lateral gaps, the lateral gaps extending from the outer lateral edges of the sidewall spacers to the inner lateral boundaries of the source/drain regions.